Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-19. (Cancelled)

20. (Currently Amended) A portion of a wrap-around-gated field-effect transistor formed on a handle wafer, the portion comprising:

an silicon-on-insulator (SOI) island comprising a surface periphery with a surface facing toward the handle wafer, the SOI island extending, for a length, along a major axis in a horizontal direction, the surface of the surface periphery and the handle wafer separated by a gap to have a non-contacting relationship; and

a gate electrode surrounding and supporting the SOI island, the gate electrode extending in a vertical direction from the handle wafer, the gate electrode having a thickness, in the horizontal direction, less than the length of the SOI island such that a first portion of the SOI island extends on one side of the gate electrode and a second portion of the SOI island extends on another side of the gate electrode, and the gate electrode extending entirely around the surface periphery of the SOI island such that a portion of the gate electrode is disposed in the gap between the surface of the SOI island and the handle wafer.

21. (Original) The portion according to claim 20, wherein a first edge face of the SOI island extends outward on one side of the gate electrode and a second edge face of the SOI island extends oppositely outward on another side of the gate electrode.

22. (Original) The portion according to claim 20, wherein the gate electrode has a cross-sectional profile that is C-shaped.

23. (Original) The portion according to claim 20, wherein a portion of a top surface of the SOI island is exposed.

24. (Original) The portion according to claim 20, wherein at least a portion of SOI island is supported underneath by an oxide layer on the handle wafer.

25. (Currently Amended) A wrap-around-gated field-effect-transistor formed on a handle wafer, the field-effect-transistor comprising:

an silicon-on-insulator (SOI) island comprising a surface periphery with a surface facing toward the handle wafer and two edge faces, the SOI island oriented substantially in a horizontal direction, the surface of the surface periphery and the handle wafer separated by a gap to have a non-contacting relationship;

a wrap-around gate electrode surrounding and supporting the SOI island, the gate electrode oriented in substantially a vertical direction intersecting with the SOI island between the two edge faces such that a first portion of the SOI island extends on one side of the gate electrode and a second portion of the SOI island extends on another side of the gate electrode, and the wrap-around gate electrode extending entirely around the surface periphery of the SOI island such that a portion of the gate electrode is disposed in the gap between the surface of the SOI island and the handle wafer;

a source region formed in the first portion of the SOI island; and

a drain region formed in the second portion of the SOI island.

26. (Previously Presented) The field-effect transistor of claim 25, wherein a portion of a bottom surface of at least one of the first portion of the SOI island or the second portion of the SOI island is exposed.

27. (Previously Presented) The field-effect transistor of claim 25, wherein at least one of the first portion of the SOI island or the second portion of the SOI island is supported underneath by an oxide layer.

28. (Cancelled)